Performance Analysis of Fir Filter Using Different Multipliers for Image Processing

Geetha K, Dr. Lakshminarayana M

Abstract— The processing of image or signal on a FPGA is the very difficult process, filters plays important role in any DSP application, the filter architecture contains the many components in that the multipliers plays an vital role ,the filter performance is mainly depends on the multiplier circuit and its performance if the multiplier circuit is complex it requires more area, more power consumption and lesser speed but the VLSI design mainly concentrates on less area, less power consumption and more speed, so to get the best solution for this problem we have choose this proposed method. This paper mainly represents the Performance analysis of a novel FIR filter for the image processing application using different multipliers and adders. The Three different types multipliers such as Booth, Vedic and Constant multipliers and adders like Ripple carry adder(RCA), carry save adder(CSA), full adder and half adder are design using verilog code. The FIR filter is designed using 8-bit Vedic multiplier and 8-bit Ripple Carry adder and Synthesized on Xilinx 14.7 and the same simulates on Modelsim, the image input for the filter is processed on matlab, and finally the comparison is made between the designed multipliers and adder based on the parameters number of LUTs and IOBs, power, path delay and maximum frequency utilized.

Index Terms— Multipliers, Adders, FIR filters, DSP, Vedic, Booth, Constant, PSNR.

1 INTRODUCTION

THE Multiplication is a very important operation in many DSP applications. In image processing filters are used to suppress the noise in images. There are mainly two types of digital filters FIR and IIR filter, FIR filters has finite duration, stable and have linear phase, FIR filters doesn't have phase distortion, but the IIR filters has the infinite duration and there stability is not guaranteed and have non linear phase, the IIR filters have the phase distortion due to this FIR filters efficient than the IIR filters. So in this project I am concentrating on designing FIR filters. Low path delay and smaller area are some of the most important criteria for the fabrication of any DSP system and other high performance systems. So optimizing the speed and area of the multiplier is a major design issue. However, area and path delays are usually conflicting constraints so that improving speed results mostly in larger areas.

In this project we try to determine the best solution for this problem by comparing a three different multipliers. In this project first designed the three different types of multipliers using Vedic multiplier (Urdhva Triyakbhyam Sutra), Booth and Constant multiplier algorithms. We used different types of adders like half adder, Full adder and Ripple carry adder to design these multipliers.

Then designed a FIR filter and in place of multiplication and addition we used the Vedic multiplier and Ripple carry adder respectively for the image processing application as to get a good PSNR valued image. We compared the working of different types of multipliers by comparing the area, path delays and power consumption of each of them. The Multipliers and adders are designed in Verilog HDL code, the FIR filter is synthesized on Xilinx 14.7 and the same is simulates on modelsim.

The main two types of filters are

1. Digital Filters
2. Analog Filters

In this paper we concentrating on Digital filters. The FIR and IIR filters are the two classes of digital filters. The term impulse response referred to the appearance of the filter in time domain. The FIR filters has linear phase, stable and have finite duration but the IIR filters have has non linear phase, it has the infinite duration and have stability issue, due to this reason in this paper we choose the FIR filter for the image processing application .Input for the proposed filter is the image the image PSNR (Peak Signal to Noise Ratio) value is calculate using the formula given below.

$$PSNR=10\log_{10}((MAXI \times MAXI)/MSE) \quad (1.1)$$

Where MAXI is the maximum value of pixel in original image MSE is the Mean Square Error.

2 LITERATURE AND REVIEW

The most recent and popularly matching research works towards the design and implementation of FIR filter using different multiplication techniques for a DSP application, design of different multipliers, application of multipliers and the role of multipliers in VLSI circuit design.

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A Review regarding the different type of multipliers and these multipliers for an efficient digital filter design for an DSP applications are discussed

2.1 Aneela Pathan, Sharmeen Keerio, In Tayab D Memon [1]

The Author has presented the paper "FPGA based performance analysis of multiplier policies for FIR filter" Authors have reviewed that the working of the different multipliers for performing multiplication in the DSP algorithms including: FFT, DCT, Euclidean distance, Signal and Image processing and as of many others till now. Therefore, computational performance of a DSP systems is measured by its multiplication operation performance. Due to the speed is considered as the key performance parameters of any circuit and the speed depends on the two things, such as clock speed of an designed circuit and number of clock cycles, which are required to perform any given task in the circuit. The traditional multipliers like sequential and array multipliers require the much hardware implementation for performing the multiplication operation. So this author focused on tradeoff of Booth and Wallace Tree multipliers architectures in multi-bit FIR filter with small commercial FPGA devices provided by the Altera, the two algorithms are more efficient in resource utilization with respect to performance compare to the traditional methods.

2.2 Laxman S [2]

The Authors have published paper on "Comparative study of Array multiplier", where the authors have been presented the array multiplier algorithm. The Algorithm Explains the detailed study of the different multipliers for all which are based on Array Multiplier in general, Constant coefficient multiplication (KCM) and multiplication based on Vedic mathematics are the major concentrated of work.

The advantage of the array multiplier is that it has a regular structure simplified the designing of the Multipliers. Another advantage of the array multiplier is its ease of design for a pipelined structure. Major disadvantage of defined array multiplier and given size. As operand increase, arrays grow in size at a rate equal to the square of the size of an operand. Which comes with the conventional multiplier.

2.3 Ruchi Sharma [3]

Presented the paper on different multiplier architectures are implemented in Xilinx FPGA and compared for their performance.

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It is a powerful algorithm when compared for the signed-number multiplication, which treats signed positive and signed negative numbers uniformly. The limitation of array multiplier speed of the multiplier is increased by the booth algorithm. Booth algorithm reduces the number of partial products. In add-shift operation each multiplier bit multiply with the multiplicand and to be added to the partial product. Major limitation of array multiplier is size. As size of an operand increase, arrays grow in size at a rate equal to the square of the operand size, hence speed of given multiplier reduces .In order to increase the speed of proposed multiplier booth algorithm is used. Booth multiplier which makes use of common Booth encoding algorithm in order to reduce the number of partial products by considering two bits of the multiplier at given a time interval, thereby achieving a speed advantage and other multiplier architectures.

2.4 Mohammed Hasmat Ali, et.al [4]

Presented the paper on "Study of Vedic Multiplier". The paper concentrated on the multiplier is based on an algorithm Urdhva Tiryakbhyam (Vertical & Crosswise). In Vedic mathematics, two of sixteen sutras are mainly used for multiplication process. Vedic multiplier gives the improved speed than the conventional multiplier and reduces the system memory. Very small area is required for this multiplier as compared to other multiplier architecture. For binary and decimal number multiplication this multiplier is used and also it is used in unsigned and signed number multiplication. The Vedic Urdhva multiplier is much more efficient than Array and Constant Coefficient Multiplier (KCM) in terms of execution time. The main Disadvantage of this multiplier is system becomes complex for complex multiplications.

2.5 Vidhi Gupta1, et.al [5]

The author have presented the paper "The Comparative study of Wallace tree multiplier". The author have introduces the Analysis and comparison of various parameters for different multiplier designed. Wallace tree is an efficient hardware implementation of a digital circuit that multiplies two integers. They are irregular in structure such that the informal description does not specify a systematic method for the compressor interconnections. It is considered as efficient implementation of adding partial products in parallel. The Wallace tree multiplier using CSA occupies smallest area while the Vedic multiplier using KSA occupies the large area. The power consumption of the four multipliers is convergent. The parallel FIR filter, Wallace tree multiplier using CSA has the minimum path delay, whereas Vedic multiplier using conventional adder has the maximum path delay.

2.6 P. Kollig, B.M. Al-Hashimi, K.M. Abbott [6]

Presented the paper "FPGA Implementation of High Performance FIR Filte.", In this paper brief about 64-tap linear phase filter operating at 1.4 MHz for given designe with 60dB attenuation at 0.28fs and 12dB attenuation at 0.25fs based on for an explicit multiplier. The presented paper provides the evidence for the pipelined multiplier provides best trade-off between speed and resource requirement

2.7 Hanho Lee, et.al [7]

Presented the paper "PGA Based FIR Filter Using Digital Serial Arithmetic". The author concentrated his work on the design of the digital-serial 5-tap FIR filter on a Xilinx XC4010 tool were FPGA is implemented. The results provide evidence for the digital-serial design with an digit-size of 2 bit have about 17% smaller area-time product than those of bit-serial implementations.

2.8 Lin Jieshan, et.al [8]

Presented the paper on "An Design of the 16-Order FIR Digital Filter Based on FPGA". The proposed paper, introduces the design and simulation of FIR filter which based on FPGA, Quartus II tool and Matlab are the tools utilized to the implementations of the Filter. Results concluded that, the use of this software significantly shortens the R& D period and it is ablelity to greatly improve the speed of the filter by use of the pipelining structure.

2.9 Asgar Abbaszadeh, et.al [9]

Author have presented the paper on "A New Hardware Efficient Reconfigurable FIR Filter Architecture Suitable for FPGA Application". The author presents hardware efficient for an reconfigurable FIR filter architecture is proposed based on binary signed sub coefficient method. Using this coefficient method the hardware requirement for the multiplexer unit is reduced with respect to typical method. The results concluded that, the FPGA synthesis results of the designed two filters based on 3-bit and 4-bit partitioning have been shown 33% and 27% reduction in the resource usage with respect to two state of art architecture.

2.10 Bahram Rashidi, et.al [10]

Presented the paper on "Low Power FPGA Implementation of Digital FIR Filter Based on Low Power Multiplexer Base Shift/Add Multiplier".The Author explains the implementation of low power and low area digital Finite Impulse Response (FIR) filter is presented. FIR filter has been synthesized, developed and designed using Xilinx ISE V7.1ISE, Virtex IV and FPGA tools. The results explains that the, minimum power can be achieved when tested power is 56mw in fir filter based on shift/add multiplier in 100MHz with 8-bit input and 8-bit coefficient.

2.11 B. Mamatha, et.al [11]

Author have presented the paper on "A New Hardware Efficient Reconfigurable FIR Filter Architecture Suitable for FPGA Application".

The author presents hardware efficient for an reconfigurable FIR filter architecture is proposed based on binary signed sub coefficient method. Using this coefficient method the hardware requirement for the multiplexer unit is reduced with respect to typical method. The results concluded that, the FPGA synthesis results of the designed two filters based on 3-bit and 4-bit partitioning have been shown 33% and 27% reduction in the resource usage with respect to two state of art architectur Presented the paper on "Design and Implementation of 120-Order FIR filter Based on FPGA". The Work conveys utility of the high speed FIR filter is implemented using registered adders and hardwired shifts and modified common sub expression which elimination algorithm is used to reduce the number of adders in the implementation. The result were tested with the help of ALTERA IDE. The results presents that, utilizing the propsed method can reduce significant area and power is reduced as compared to general Distributed Arithmetic technique.

2.12 Mrs. Pooja, et.al [12]

Presented the paper on "High Speed Vedic Multiplier in FIR Filter on FPGA". In paper presented is based on FIR filter and its designed using fast method for multiplication based on Vedic mathematics. The multiplication is based on Urdhava Tiryakbhgyam sutra. At the end paper conclude that Vedic multiplier can achieves high speed by reducing gate delays and the Urdhava Tiryakbhagyam method is more efficient than conventional method

2.13 Vijender Saini, et.al [13]

Presented the paper on "Area Optimization of FIR Filter and its Implementation on FPGA". Paper Presents will explain about multiplication with Canonical Sign Digit (CSD) and binary number is simulated and implemented on the Spartan3E devices. In the presented paper area in terms of number of slices is optimized by 80% in Canonical Sign Digit Algorithm

2.14 Jhasi, B. R.et.al [14]

Presented the paper on "Design and Analysis of High Performance FIR Filter Using MAC Unit". The paper provide over view of FIR filter with better performance using low power adder and multiplier. The carry skip adder (CSA) included with modified Wallace tree multiplier consumes low power among all adders and multiplier circuit and tested result. The result of FIR filter consumes less power than the conventional FIR filter

2.15 Kazi Nikhat Parvinc [15]

Presented the paper "Multiplication Techniques for an Efficient FIR Filter Design for Hearing aid Applications." The author provides brief study of designing and Implementation of a Low pass FIR filter of order 10. Author provide the justify that utilized frequencies are that of hearing aid application. To filter the optimized area of different multiplication Techniques such as constant multiplier and booth multiplier and modified booth multiplier and vedic multiplier have been used to multiply filter coefficient of input, The tested constant multiplier is efficient in the Direct form structure where as in trans-

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pose form modified booth has maximum frequency and area consumed is relatively low

3 Conclusion

From the above literature survey it is concluded that the multipliers is the one of the most important component to design an efficient filter and FIR filter is the most important element in Digital Signal Processing (DSP) application such as video, Image processing and other wireless communication. So we proposed a survey mainly concentrating on the study of different methods for designing the different multipliers to design of an efficient FIR filter to get efficient filter output. Future work will be concentrated on the designing of three different multipliers such as Vedic Multiplier and Booth Multiplier and Constant Multiplier and designing of the adders like 8-bit ripple carry adder, 8-bit full adder and half adder, and then designing of the FIR filter in direct form structure using 8-bit Vedic multiplier and 8-bit ripple carry adder respectively for the image processing application as to get an good PSNR valued image and finally the comparison is made between the designed three multipliers based on some of the parameters such as area, path delay, maximum frequency used and speed.

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